Laminate Al_2O_3/Ta_2O_5 Metal/Insulator/Insulator/Metal (MIIM) Devices for High-Voltage Applications

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***Abstract*— We evaluate for high-voltage (HV) applications a series of metal/insulator/insulator/metal (MIIM) devices with relatively thick asymmetric Al_2O_3/Ta_2O_5 bilayer insulator barriers in which the Al_2O_3:Ta_2O_5 layer thickness ratio is varied from 1:1 to 1:9, with the thickness of the Al_2O_3 layer fixed at 30 nm. The impact of Ta_2O_5 to Al_2O_3 stack order and layer thickness ratio on current versus voltage asymmetry, reverse leakage, breakdown, and programable resistance ratio is investigated. Regions of operation are distinguished, and the responsible underlying dominant conduction mechanisms, including Schottky emission over the various barriers, ohmic conduction and Fowler–Nordheim tunneling through Al_2O_3, and defect-based Frenkel–Poole emission through Ta_2O_5 are identified. It was found that under positive bias, the low-resistance state in one-time programable usage is controlled by the thickness and properties of the Ta_2O_5 layer while the high-resistance state is determined by the thickness and properties of the Al_2O_3 layer. These results demonstrate that atomic layer deposition (ALD) bilayers are an effective way to engineer the electrical properties of HV metal-insulator-metal (MIM) devices.**

***Index Terms*— Al_2O_3, atomic layer deposition (ALD), conduction mechanisms, laminate, metal/insulator/metal (MIM), metal/insulator/insulator/metal (MIIM), MIM diode, Ta_2O_5.**

I. Introduction

BACK-END-OF-LINE (BEOL) metal-insulator-metal (MIM) devices, such as capacitors and resistive random access memory (RRAM), help to increase integrated circuit packing density by multilevel stacking of devices. Recently, thin-film MIM tunnel diodes have gained widespread interest for a number of applications, such as rectification for solar rectenna-based energy harvesting [1]–[4], infrared (IR) detection, selector diodes for RRAM [5], hot-electron transistors [6], [7], single-electron transistors [8], and field emission cathodes [9]–[11]. Typically, the current versus voltage performance of single insulator MIM devices is controlled by the built-in electric field induced by the work function difference ($\Delta\Phi_M$) between the two dissimilar metal electrodes, which is limited to a maximum of roughly 1.3 eV for practical materials [12], [13]. Recent work, however, has demonstrated that engineering the asymmetry of the tunnel barrier by using asymmetric bilayer and multilayer nanolaminate heterostructure insulators with different electron affinities is a more effective way to optimize these devices. Furthermore, by properly aligning the asymmetric tunnel barrier with $\Delta\Phi_M$, one can greatly improve the asymmetry ($\eta_{asym} = |J^-/J^+|$,), nonlinearity ($f_{NL} = (dJ/dV)/(J/V)$), responsivity ($(1/2)(d^2J/dV^2)/(dJ/dV)$), and zero-bias-resistance of these devices ($J/V|_{V=0\,V}$) [7], [14]–[24]. Work on dual insulator-metal/insulator/insulator/metal (MIIM) devices to date have focused on thin-films insulator stacks for low voltage applications. For example, it was recently shown that the use of 5-nm-thick Ta_2O_5/Al_2O_3 bilayers with TaN bottom and Al top electrodes, resulted in $\eta_{asym} > 10$ and f_{NL} of ~5 at less than 0.5 V, a significant improvement over Ta_2O_5 or Al_2O_3 alone [18]. There is also an interest in using MIIM-based devices for high-voltage applications, such as diodes for circuit routing optimization, energy management for flexible wearable electronics, high-voltage logic, antenna diodes for plasma-induced damage (PID) and electrostatic discharge protection, and antifuse one-time programable (OTP) nonvolatile memory [25]–[27]. Based on oxide breakdown, antifuse OTP memory is a class of programable read-only memory (PROM) that can be programed only once. Because of its low leakage in the nonprogramed state, relatively small readout voltage, and imperviousness to altering the state of the device with heat or voltage, they are in demand not only for analog/sensor trimming and calibration, but also for high-security applications, such as secure key storage and device IDs [28].

In this article, we evaluate a series of thick (60–300 nm) Al_2O_3/Ta_2O_5 bilayer MIIM devices for high-voltage applications and investigate the impact of Ta_2O_5 to Al_2O_3 stack order and layer thickness ratio on device performance, including asymmetry, reverse leakage, breakdown, and programable resistance ratio. Regions of operation are distinguished,

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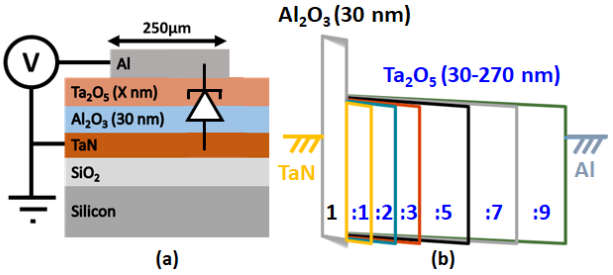

Fig. 1. (a) Schematic cross-section and (b) superimposed equilibrium band diagrams for Al/Ta_2O_5/Al_2O_3/TaN MIIM devices.

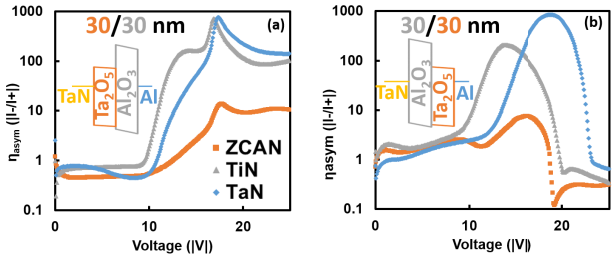

Fig. 2. Plots of log (η_{asym}) versus |*V*| for (a) Ta_2O_5/Al_2O_3 and (b) Al_2O_3/Ta_2O_5 MIIM diodes, each with Al top electrodes and either TaN, TiN, or ZrCuAlNi bottom electrodes.

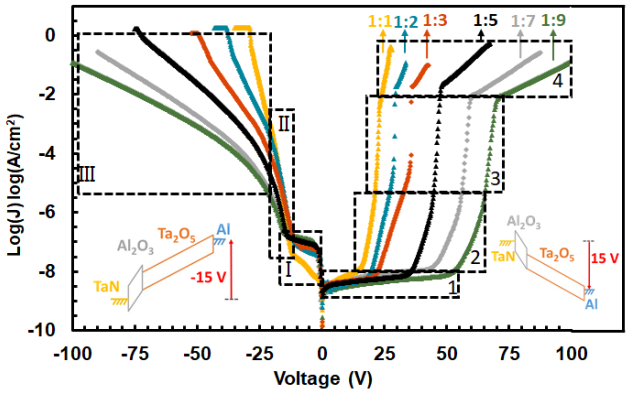

Fig. 3. Representative log *J* versus *V* curves for a series of TaN/Al_2O_3/Ta_2O_5/Al MIIM devices with constant Al_2O_3 thickness (30 nm) and varying Ta_2O_5 thickness, with Al_2O_3:Ta_2O_5 thickness ratios labeled. Three distinct conduction regions are indicated for negative bias (labeled I, II, III, and demarcated with dashed lines) and four conduction regions are indicated for positive bias (labeled 1 through 4 and demarcated with dashed lines). Inset: negative and positive bias band diagrams for the 1:5 device.

underlying dominant conduction mechanisms are identified, and performance is evaluated for OTP applications.

II. Experimental

Dual insulator Al_2O_3/Ta_2O_5 MIIM diodes were fabricated using three different substrates as bottom electrodes. The majority of the work was performed using Si/SiO_2/Ta/TaN substrates with the TaN layer planarized via chemical mechanical polishing (provided by ON Semiconductor). For comparison, Si/SiO_2 substrates with either sputtered ZrCuAlNi or sputtered TiN were also investigated. Atomic layer deposition (ALD) of Al_2O_3 and Ta_2O_5 was performed at 200 °C in a Picosun SUNALE R-150 reactor using alternating N_2-purge-separated pulses of H_2O and either trimethylaluminum (TMA) or tris(ethylmethylamido)(tert-butylimido)tantalum(*V*) (TBTEMTa), respectively. The TMA and TBTEMTa sources were held at 17 °C and 90 °C, respectively. The deposition rates of Al_2O_3 and Ta_2O_5 were approximately 0.092 and 0.051 nm/cycle, respectively. Al_2O_3/Ta_2O_5 bilayer stacks were deposited without breaking the vacuum. For completing the fabrication of MIIM diodes, 250-μm-diameter Al top contacts (an area of approximately 0.05 mm^2) were thermally evaporated through a shadow mask. A schematic cross section of a TaN/Al_2O_3/Ta_2O_5/Al MIIM diode is shown in Fig. 1(a).

Insulator film thickness was measured using a Woollam M2000 variable angle spectroscopic ellipsometer (VASE) in the wavelength range of 400–1000 nm. Current versus voltage measurements were taken using an Agilent B1500A in the dark with the bottom electrode held at ground. Measurements were performed on pristine devices with the bias swept from 0 V to the maximum absolute voltage, with new devices used for each polarity. The area of each Al contact was measured (with an average error of ±1.8%) for area normalizations.

III. Results and Discussion

A. Deposition Temperature, Layer Order, and Lower Electrode

To obtain the maximum asymmetry of MIIM diodes with 30 nm/30 nm (1:1 ratio) Al_2O_3/Ta_2O_5 insulator stacks, three parameters are varied: 1) the ALD temperature (200 °C vs. 250 °C); 2) the bottom electrode (TaN, TiN, and ZrCuAlNi); and 3) the order of insulator deposition (Al_2O_3/Ta_2O_5 vs. Ta_2O_5/Al_2O_3). For all devices, an ALD temperature of 200 °C produces a greater maximum asymmetry than a temperature of 250 °C. Shown in Fig. 2 are η_{asym} versus V plots for all of the 200 °C deposited devices. Of the three bottom electrode metals, TaN has the greatest asymmetry for all ALD temperatures and insulator orientations, indicating that TaN has a larger effective work function with both Al_2O_3 and Ta_2O_5 than does either TiN or ZrCuAlNi. Finally, an insulator orientation of TaN/Ta_2O_5/Al_2O_3/Al shows the greatest asymmetry in all cases except for devices with a TaN bottom electrode. This same orientation with respect to the electrode work functions also led to the largest asymmetry in our previous report on ultrathin Al_2O_3/Ta_2O_5 stacks [18]. Subsequent experiments were, thus, performed on TaN substrates with an insulator orientation of Al_2O_3/Ta_2O_5 and an ALD temperature of 200 °C.

B. Conduction Mechanism Analysis

Superimposed equilibrium band diagrams (generated using software [29] with bandgaps and permittivities from [13]) for a series of Al_2O_3/Ta_2O_5 MIIM devices with the Al_2O_3 layer fixed at 30 nm and the Ta_2O_5 layer thickness varied from 30 to 270 nm, such that the Al_2O_3:Ta_2O_5 thickness ratio is varied from 1:1 to 1:9, is shown in Fig. 1(b). Plots of logarithmic current density versus applied voltage (*J*–*V*) for these devices (Fig. 3) reveal that the Al_2O_3:Ta_2O_5 thickness ratio affects the *J*–*V* characteristics in a number of distinct ways for positive and negative bias.

1) Positive Bias: Under positive bias, four distinct regions of *J*–*V* behavior are apparent (marked 1–4 in Fig. 3). In each of these regions, the dominant conduction mechanisms are determined using a combination of *J*–*V* simulation, linearization of test data, and elevated temperature testing (where appropriate).

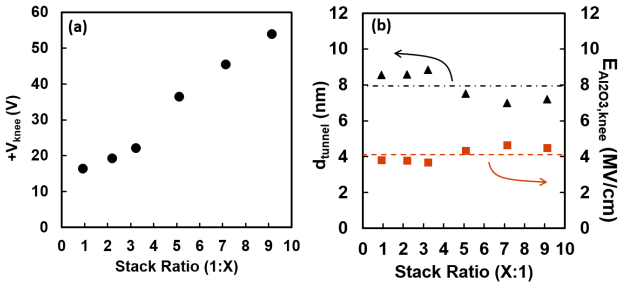

Fig. 4. (a) Plot of positive V_{knee} versus Al_2O_3:Ta_2O_5 thickness ratio. (b) Plot of $E_{Al2O3,knee}$ (right-hand axis, orange squares) and d_{tunnel} (left-hand axis, black triangles) in Al_2O_3 versus Al_2O_3:Ta_2O_5 thickness ratio assuming an ideal capacitive voltage divider. The average value for each quantity is indicated with a horizontal dashed line.

Region 1 is defined as the region prior to the "knee" in each J–V curve that marks the onset of steeply increasing conduction. As an example, for the 1:5 device, Region 1 begins at 0 V and ends at approximately 37 V. Within this region, J is linearly dependent upon V, suggesting ohmic conduction where

$$J_{\text{ohmic}} = nq\mu E \tag{1}$$

and where n is the density of electrons in the conduction band (CB) of the insulator, q is the elementary charge, μ is the electron mobility within the insulator, and E is the electric field in the insulator. Fitting (1) to the linearized J–V data yields a mobility μ of roughly 20 $cm^2/(V\ s)$ and an n of roughly 3×10^3 cm^{-3}, both reasonable values for Al_2O_3, indicating that ohmic conduction through the Al_2O_3 is the likely dominant charge transport mechanism in Region 1.

Region 2 is defined between the "knee" (again, occurring at roughly 37 V for the 1:5 device) and the more subtle increase in slope (occurring at approximately 44 V for the 1:5 device). This region is well described by Fowler–Nordheim tunneling (FNT), an electrode/interface-controlled conduction mechanism in which electrons quantum mechanically tunnel through the triangular barrier formed when a high electric field is applied across the insulator tunnel barrier. FNT is distinct from direct tunneling, in which electrons must tunnel through the entirety of the insulator thickness, and may be described as

$$J_{\text{FNT}} = \frac{q^3E^2}{16\pi^2\hbar\varphi_{Bn}} \exp\left[-\frac{4\sqrt{2m_e^*}\varphi_{Bn}^{3/2}}{3hE}\right] \tag{2}$$

where $\hbar$ is the reduced Plank's constant, φ_{Bn} is the barrier height between the two materials of interest (in this case, the TaN/Al_2O_3 interface), and m_e^* is the electron effective mass in the insulator [30]. Linearizing this equation and replotting Region 2 of Fig. 3 as $\ln(J/E^2)$ versus $1/E$ allows an assessment of the likelihood of FNT (through the determination of the R^2 value of a linear fit). Good fits ($R^2 > 0.994$) are observed for the all of the devices, strongly suggesting that FNT through the Al_2O_3 layer is limiting charge transport in Region 2.

The voltage at which the knee occurs (V_{knee}) increases roughly linearly with increasing stack ratio from roughly 16 V for the 1:1 to roughly 54 V for the 1:9 devices, as shown in Fig. 4(a), where the knee values are determined from the intersection of the slopes of the pre-knee and post-knee regions.

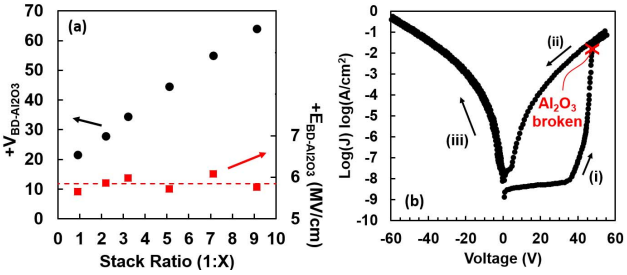

Fig. 5. (a) Plots of $V_{BD,Al2O3}$ and $E_{BD,Al2O3}$ for all devices under positive bias. The average of the $E_{BD,Al2O3}$ of all device types is indicated by the horizontal dashed line. (b) Plot of J–V sweep following breakdown of the Al_2O_3 under positive bias.

Assuming that the devices behave as ideal capacitive voltage dividers under positive applied bias, the electric field present across the Al_2O_3 layer ($E_{Al2O3,knee}$) and effective tunneling distance (d_{tunnel}) through the Al_2O_3 layer are calculated at V_{knee} and plotted for each device in Fig. 4(b). The average of the $E_{Al2O3,knee}$ and d_{tunnel} across all thickness ratio devices is 4.0 MV/cm and 8.1 nm. Although there does appear to be a slight difference between the average values for the three low ratio stacks versus the three high ratio stacks, this may be an extraction artifact due to the increased contribution of Frenkel–Poole emission (FPE) conduction in stacks with thinner Ta_2O_5 layers. Extrapolation of the three lowest ratio and three highest ratio stacks in Fig. 4(a) to the y-axis (zero Ta_2O_5 layer thickness) both yield $V_{knee} = 12$ V ($E_{Al2O3,knee} = 4$ MV/cm), consistent with the average of the calculated values and with previous reports of electric field for FNT onset in Al_2O_3. The FNT linearization, $E_{Al2O3,knee}$ values, and d_{tunnel} values taken together, indicate that Region 2 is dominated by FNT through the Al_2O_3 layer.

Again referring to Fig. 3, Region 3 is bounded at lower voltages by the subtle increase in slope and at a higher voltage by the abrupt decrease in slope. Following FNT conduction through the Al_2O_3 in Region 2, as the voltage is increased, the field across the Al_2O_3 layer eventually reaches the breakdown strength, and irreversible hard breakdown occurs. The voltage at the onset of breakdown (V_{BD}) for each device is plotted in Fig. 5(a). Again by assuming an ideal Al_2O_3/Ta_2O_5 capacitive voltage divider, the electric field in the Al_2O_3 layer at which hard breakdown occurs ($E_{BD,Al2O3}$) is calculated for each device and plotted in Fig. 5(a) for all stack ratios. The calculated $E_{BD,Al2O3}$ is roughly independent of stack ratio, and the average $E_{BD,Al2O3}$ for all device types, is roughly 5.8 MV/cm. Extrapolating the $V_{BD,Al2O3}$ data to the y-axis (zero Ta_2O_5 thickness) yields ~18 V or ~6 MV/cm, consistent with the average of the calculated values.

Finally, Region 4 of the positive bias response in Fig. 3 is marked by the abrupt decrease in slope following the breakdown of the Al_2O_3 layer. Once a breakdown occurs, and the device enters Region 4, the J–V behavior is irreversibly changed, as shown in Fig. 5(b). Subsequent current-voltage behavior is limited by FPE through only the Ta_2O_5 layer, described by

$$J_{\text{FPE}} = q\mu N_C E \exp\left[\frac{-q(\varphi_T - \sqrt{qE/(\pi\varepsilon_r)})}{kT}\right] \tag{3}$$

where N_c is the density of states in the CB, E is the electric field in the Ta_2O_5, φ_T is the energy level of the traps through

which FPE conduction occurs, ε_r is the optical dielectric constant of the insulator, and k is Boltzmann's constant [30]. FPE conduction in similarly deposited Ta_2O_5 was previously seen in [31]; fitting of FPE conduction for Region III will be discussed below.

2) Negative Bias: For negative bias operation, three distinct conduction regions are apparent (marked I, II, and III in Fig. 3). The initial negative sweep in Region I shows a rapid increase in current to about 10^{-7} A/cm^2 followed by a rough "shelf" of slowly increasing current versus voltage. In subsequent negative sweeps (not shown), current density remains low to about -3 V before rapidly increasing to the same "shelf" value. The negative shift in the voltage at which the rapid increase in current occurs is likely due to the charging of defects at the Al_2O_3/Ta_2O_5 interface or in the Ta_2O_5.

For the 1:1 device, the J–V response in Region I shows a high degree of linearity for Schottky emission (SE), where

$$J_{\mathrm{SE}} = A^* T^2 \exp\left[\frac{-q(\varphi_{Bn} - \sqrt{qE/(4\pi\varepsilon_r)})}{kT}\right] \tag{4}$$

where A^* is the effective Richardson constant for the insulator into which the electron is being injected [30]. Fitting is achieved by replotting data from Region I as $\ln(J)$ versus $E^{1/2}$ and calculating the coefficient of determination (R^2) for the region of interest. For the 1:1 device, the Region I shelf is highly linear ($R^2 = 0.998$) indicating that SE is likely the dominant conduction mechanism. Under negative bias, there are two energy barriers to be surmounted, the Ta_2O_5/Al barrier with a theoretical ideal value of 1.0 eV, and the Al_2O_3/Ta_2O_5 barrier with an ideal value of 1.8 eV (assuming a steady supply of electrons in the Ta_2O_5 CB). As one would expect that the larger barrier would be the limiting factor in charge transport, we tentatively assign SE over the Al_2O_3/Ta_2O_5 barrier as the dominant conduction mechanism for the 1:1 device. As expected for SE, we observed through separate measurements (not shown) that the current exhibits temperature dependence.

With increasing Al_2O_3:Ta_2O_5 ratio, current density increases, and the R^2 value for SE in Region I decreases, suggesting that another conduction mechanism is playing a increasingly important role. For all devices, it is presumed that charge from the Al top electrode is injected into the Ta_2O_5 via either SE over the Ta_2O_5/Al barrier or direct tunneling into the abundant defect levels at about 0.5 eV below the CB of Ta_2O_5 [13]. In the Ta_2O_5, charge transports rapidly through these defect levels via FPE. Upon reaching Al_2O_3/Ta_2O_5 interface, there will be SE of charge over the Al_2O_3/Ta_2O_5 barrier. For the higher ratio devices, however, the increased current flow indicates that there must be an additional conduction path.

One possible contribution of additional current is from hot carriers. As the thickness ratio is increased to 1:2 and above, for the same applied voltage range, the CB of Ta_2O_5 begins to rise higher than the CB of Al_2O_3. This situation creates the potential for hot electrons within a mean free path of the interface to either surmount the Al_2O_3/Ta_2O_5 barrier and be directly injected into the CB of Al_2O_3 or to energetically assist with SE. As there is a large increase in current between the 1:1 and 1:2 stacks, but only small increases for thicker stacks, it may be that only electrons within a narrow band of distance (at the edge of the mean free path) away from the interface

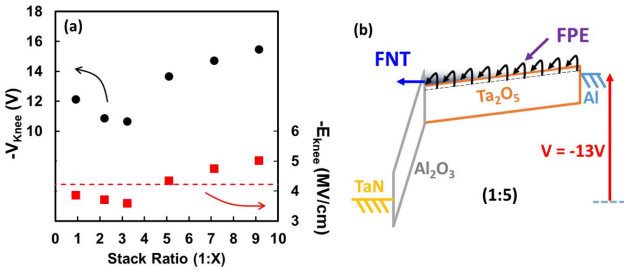

Fig. 6. (a) Plot of voltage and field within the Al_2O_3 (assuming an ideal voltage divider) at which the negative knee between Regions I and II occurs for all stack ratio devices. (b) Band diagram depicting FNT in the Al_2O_3.

are hot-electron assisted, whereas closer electrons are blocked by the barrier and those farther away are thermalized.

Another, perhaps potentially more likely cause of the increase in current density with increasing insulator thickness is a negative charge at the Al_2O_3/Ta_2O_5 interface. This buildup of charge would increase the field across the Al_2O_3 and decrease the field across the Ta_2O_5, leading to increased Schottky lowering of the Al_2O_3/Ta_2O_5 barrier for thicker stacks and a concomitant increase in SE current.

Since the two interfaces are in series electrically, both hot carrier assistance and negative charge buildup would shift current limiting from the Al_2O_3/Ta_2O_5 to the Ta_2O_5/Al interface. Thus, for the thinner stacks, the current is limited primarily by the Al_2O_3/Ta_2O_5 interface, while for the thicker stacks, the current becomes more limited by the Ta_2O_5/Al interface. Given that injection of current at the Ta_2O_5/Al interface should remain relatively constant for all stacks, this would create an interesting situation, in which the low field current is greater for the thicker stacks than for the thinner stacks. However, due to the difficulty of modeling the competing conduction mechanisms, our assessment of conduction in this region is inconclusive.

The start of Region II (Fig. 3) is characterized by a knee marking a steep slope change to exponentially increasing current, which we assign to the onset of FNT through the Al_2O_3 barrier. Due to high defect density, thermal conduction mechanisms, such as FPE, typically overwhelm tunneling in Ta_2O_5, as demonstrated in Region 4 for positive bias [31].

Shown in Fig. 6(a) is a plot of the negative onset voltage for FNT through the Al_2O_3 ($-V_{\mathrm{onset,FNT}}$) for each ratio device, as determined from the intersection of pre-knee and post-knee slopes. A band diagram illustrating device operation in this regime is shown in Fig. 6(b). While $+V_{\mathrm{onset,FNT}}$ is a strong function of the stack thickness, as expected for a capacitive voltage divider [Fig. 5(a)], under negative bias, $-V_{\mathrm{onset,FNT}}$ occurs at lower absolute voltages and is only a weak function of stack thickness. Assuming the devices act as ideal capacitive voltage dividers under negative bias, the onset field across the Al_2O_3 layer, $E_{\mathrm{onset,FNT,Al2O3}}$, *decreases* from roughly -2.7 MV/cm for the 1:1 to roughly -1.25 MV/cm for the 1:9 device. Not only is this field, in all cases, too low to account for FNT in Al_2O_3, $E_{\mathrm{onset,FNT,Al2O3}}$ should be roughly the same for all stack ratios because the Ta_2O_5/Al_2O_3 barrier heights remains the same, as do the properties of the Al_2O_3. This indicates that the ideal capacitive voltage divider model does not hold for negative bias. Due to high levels of FPE conduction, the Ta_2O_5 layer is highly con-

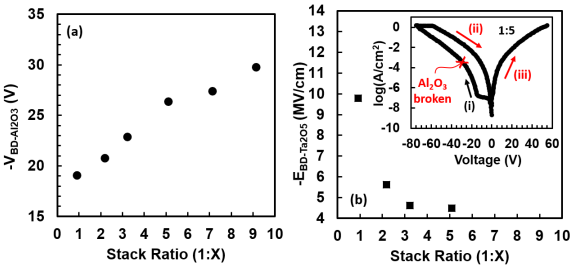

Fig. 7. Plot of (a) applied voltage at which breakdown of the Al_2O_3 layer occurs and (b) field within the Ta_2O_5 at which negative breakdown of Ta_2O_5 occurs for those ratio devices which exhibit this behavior. Inset: reverse sweep for the 1:5 device taken after negative breakdown showing that the Al_2O_3 no longer contributes to the current-voltage behavior.

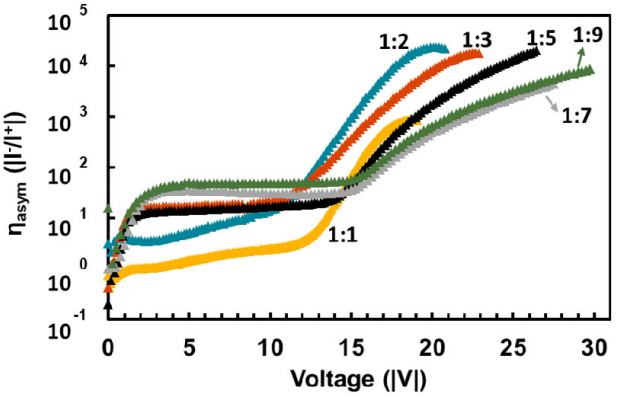

Fig. 8. Plots of achievable log (η_{asym}) versus $|V|$ for all devices, plotted up to the negative breakdown voltage of the Al_2O_3 layer.

ductive compared to the Al_2O_3. Therefore, under negative bias, the insulator stack may act more as a resistive voltage divider, such that most of the voltage drop is across the Al_2O_3 layer.

If we simply assume that all of the voltage drops occur across the Al_2O_3, we find that $-E_{onset,FNT,Al2O3}$ is roughly constant at -4 MV/cm for all device stacks [see Fig. 6(a)]. This is comparable to the roughly $+4$ MV/cm onset field for FNT through the 30-nm Al_2O_3 layer under positive bias (Fig. 4). However, there is a slight trend to higher $-E_{onset,FNT,Al2O3}$ for larger insulator ratio devices. This may be accounted for by the fact that thicker Ta_2O_5 layers will have a higher series resistance and proportionally drop more of the field than thinner Ta_2O_5 layers.

The onset of Region III in Fig. 3 is marked by a distinct rollover in the slope of the J–V response. The rollover occurs due to the dielectric breakdown of the Al_2O_3 layer [inset Fig. 7(b)], resulting in the current no longer being limited by FNT through the Al_2O_3. Instead, conduction in this region is well modeled by FPE through the Ta_2O_5 layer only, with thicker layers showing higher resistance. FPE simulation using an optical dielectric constant of 4.6, a trap depth of 0.71 eV, and electron mobility of 170 cm^2/V$-$s yields a close match to the 1:5 device J–V response. The negative bias breakdown voltages [Fig. 7(a)] are much lower than observed for positive bias (Fig. 4) and have a weaker dependence on the stack thickness, increasing from roughly -17 V for the 1:1 device to $\sim$30 V for the 1:9 device. If we assume simply that all of the voltage drop occurs across the Al_2O_3 layer, we estimate a negative breakdown field ($-E_{BD,Al2O3}$) of roughly -6 MV/cm for the 1:1 device, slightly higher than $+E_{BD,Al2O3}$, likely due to the built-in field imposed by the different electrode materials. For the higher ratio devices, an increasingly greater fraction of the voltage drop will occur across the Ta_2O_5 layer due to the increase in thickness.

Finally, for the 1:1, 1:2, 1:3, and 1:5 stacks, an increase in slope is observed at larger negative biases (Fig. 3). The increased slope is due to the dielectric breakdown of the Ta_2O_5 layer, and the current quickly reaches compliance. Assuming that all of the field is dropped across the Ta_2O_5, this leads to a breakdown field of a little over 4 MV/cm, consistent with Ta_2O_5. The 1:1 device shows a larger calculated breakdown field than the thicker stacks [Fig. 7(b)] because the small voltage drop occurring across the broken 30-nm Al_2O_3 layer that is ignored in this treatment comprises a greater percentage of the total voltage drop for the lower ratio devices.

C. Device Operation

Shown in Fig. 8 is a plot of η_{asym} versus $|V|$ for all devices. For device operation at voltages less than about $\pm$12 V (below the onset of negative bias FNT through the Al_2O_3 layer), we find that η_{asym} increases roughly with increasing stack ratio from roughly 5 for the 1:1 to roughly 50 for the 9:1. In this region, the devices may be operated as a BEOL weakly rectifying MIM diode in which the asymmetry can be tuned with the thickness of the Ta_2O_5 layer.

With the onset of negative bias FNT conduction through the Al_2O_3 layer, η_{asym} increases steeply. In this region, with the exception of the 1:1 device, η_{asym} becomes higher for thinner devices. Diode operation in this region is limited by the negative bias breakdown voltage of the Al_2O_3 layer (Region III), which increases only weakly with increasing Ta_2O_5 thickness (Fig. 7). $\eta_{asym,max}$ occurs roughly at the forward (negative) breakdown voltage (at which point all plots are stopped) and, with the exception of the 1:1 devices, is roughly independent of stack thickness. The maximum asymmetry voltage is tuned by the Ta_2O_5 thickness, increasing from $\sim$19 V for the 1:1 ratio device to $\sim$52 V for the 1:9 ratio (Fig. 4).

Next, we consider the more interesting case of operation as an OTP antifuse in which the devices are operated only in reverse (positive) bias. The programing voltage, which normally is at or slightly above the circuit operational voltage, is set by the Al_2O_3 film thickness and stack ratio. In the unprogramed state, the antifuse is in the open high resistance state (HRS), and current density is very low ($<10^{-8}$ A/cm^2) up to the onset of FNT. The device is programed by ramping to the positive Al_2O_3 breakdown voltage so that the antifuse is shorted and the device is in the low resistance state (LRS), yielding a maximum programable resistance ratio (R^+_{LRS}/R^+_{HRS}) at $+V_{onset,FNT,Al2O3}$ which is controlled by the resistive properties of the Ta_2O_5 layer. For the 1:5 stack, $R^+_{LRS}/R^+_{HRS} = \sim 7 \times 10^5$ at $+V_{onset,FNT,Al2O3}$ [see Fig. 5(b)].

The maximum operating voltage in the HRS ($+V_{onset,FNT,Al2O3}$) and the reverse program voltage ($+V_{BD,Al2O3}$) may be tuned not only with the thickness of the Al_2O_3 layer but also the thickness of the Ta_2O_5 layer. The resistance of the LRS is controlled by the thickness and properties of the Ta_2O_5 layer, while the resistance of the HRS is determined by the thickness and properties of the Al_2O_3 layer.

IV. Conclusion

Using TaN bottom gates and Al top gates, a series of thick Al_2O_3/Ta_2O_5 bilayers were deposited via ALD with the Al_2O_3 layer thickness fixed at 30 nm and Ta_2O_5 varied from 30 to 270 nm to assess the impact of insulator thickness ratio on MIIM devices under high-voltage operation. Due to low-temperature fabrication, MIM-based devices are of interest for large-area electronics and in the CMOS BEOL as a way to implement 3-D integration and reduced interconnect routing conflicts, building upward away from Si.

Device operation is found to be a strong function of the Al_2O_3/Ta_2O_5 thickness ratio. Trends in conduction and η_{asym} are explained by the asymmetric barrier (Fig. 1) created by the pairing of Al_2O_3 and Ta_2O_5 and involve the interplay of several distinct positive and negative bias conduction regions, dominated by either SE, ohmic conduction and FNT through the Al_2O_3 barrier, and defect-based FPE conduction through the Ta_2O_5. Because the FNT onset voltage is dependent (independent) on the Ta_2O_5 thickness under positive (negative) bias, controlling the Ta_2O_5 thickness can effectively tune the device operation.

As an OTP antifuse, this device shows very low leakage in nonprogramed state, has a high programable resistance ratio, can be read with a relatively small voltage, is compatible with CMOS processes, scalable, reliable (once it has experienced hard breakdown, the Al_2O_3 layer will not self-heal as with e-fuse technology), and is potentially secure. As such, it is of interest for applications such as secure key storage, device IDs, and analog/sensor trimming and calibration.

This article demonstrates that ALD bilayers may be used to effectively engineer the reverse breakdown programing voltage, maximum programable resistance ratio, I–V asymmetry, and operating range of high-voltage MIM devices.

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